PART OF CPS JK25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SUPPORTING INFORMATION CURRENT DRAIN USED ON NOTES SYMBOL RECORD OF CHANGES	1	1
CIRCUIT PACK SCHEMATIC	2	1
	3	1
COMPONENT LIST	4	1
CIRCUIT DESCRIPTION TIMING	5	1

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PROCEEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. POWER AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	GRD. TERM.	BAT. TERM		
41U	8	16		
41BP	8	16		
41BU	8	16		
41CA	8	16		
KS-21285,L24	8	16		
KS-21285,L45	7	14		
KS-21286,L3	8	16		
KS-21688,L3	7	14		
KS-21827,L15	7	14		
KS-22036,L1	7	14		

3. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

4. TERMINALS 203 AND 304 ARE RESERVED AND SHALL NOT BE USED.
5. (SEE SKETCH AT LEFT).
6. CURRENT DRAIN: 680 mA

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	3-2-78	AS TLB	AR M JOE MG

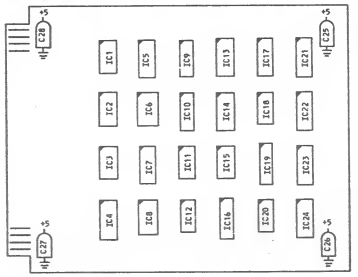
SYMBOL

FANOUT BOARD
ELEMENT A

TERM.MOD	FUNCT	TERM.	LOC	TERM.MOD	FUNCT	TERM.	LOC
AP17,01	I	305	2A8	RSEL1	B	013	2H9
AP7,01	I	204	3A9	SELRCO	B	210	2H9
AC021	I	010	3A7	SELRWO	B	205	2H1
AO111	I	112	3A7	TAPERO	B	212	3H3
AG211	I	011	3A6	UNSELERO	B	211	2H5
AO931	I	111	3A0	+5	P	000	2H2
AO421	I	207	3A6	+5	P	119	2H2
AO511	I	012	3A6	GRD	G	004	2G8
AO611	I	306	3A5	GRD	G	005	2G8
AO711	I	208	3A5	GRD	G	008	2G8
AO831	I	309	3A2	GRD	G	104	2G8
AO911	I	307	3A0	GRD	G	107	2G8
A1011	I	305	3A1	GRD	G	200	2H2
A1121	I	206	3A5	GRD	G	319	2H2
A1221	I	110	3A4				
A1321	I	308	3A4				
A1421	I	209	3A4				
A1511	I	016	3A1				
A1621	I	117	3A1				
A1721	I	019	3A3				
RASIO	I	201	2A4				
REFIO	I	214	2A5				
RWIO	I	300	2A0				
SELOI1	I	113	2A2				
TS111	I	216	2A6				
CEAO1	2B	102	3G8				
CEA11	3B	009	3H7				
CEA21	3B	109	3H7				
GCA50	2B	310	2H6				
GRA50	2B	003	2H4				
GRCA00	3B	007	3H4				
GRCA10	2B	105	3H5				
GRCA20	2B	005	3H5				
GRCA30	3B	103	3H4				
GRCA40	3B	101	3H1				
GRCA50	2B	002	3H1				
GRCA60	2B	106	3H0				
GRA0	2B	001	2H0				
MSELO	0	311	2H1				
MSELOO	2B	115	2H2				
REFDN1	2B	218	2H4				
REFO	2B	108	2H5				

NOTES: (CONT)

5. DIPS TO BE NUMBERED IN THE MANNER SHOWN BELOW (BOARD SHOWN FROM COMPONENT SIDE).



SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

SUPPORTING INFORMATION	
CATEGORY	NUMBER
CONNECTOR ON FRAME	
CIRCUIT PACK INFORMATION DRAWING	
SERIES FOR LATEST CLASS "A" CHANGE	
ACCEPTABLE SERIES	

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

INMB

AT&T ACO STANDARD

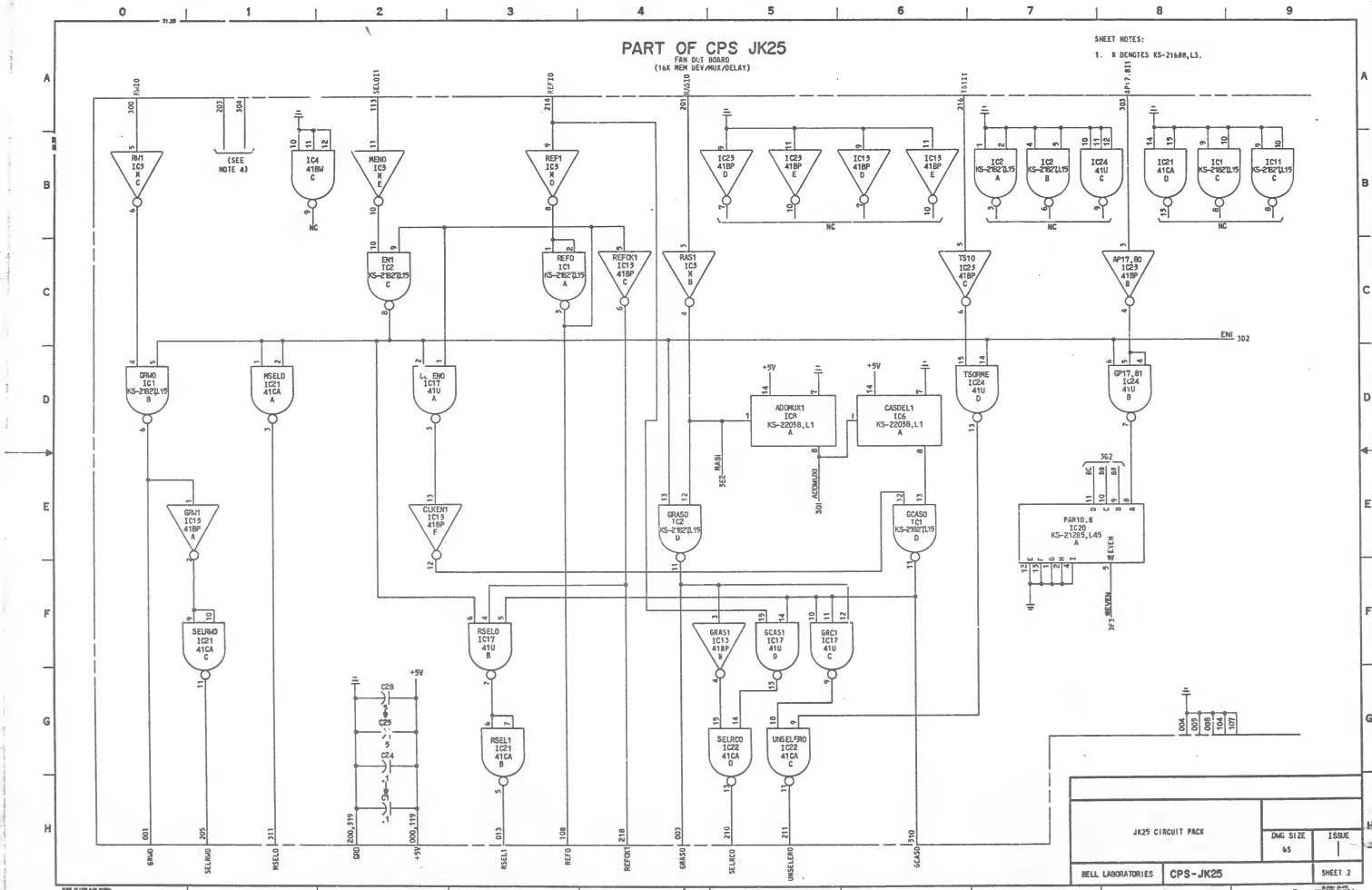
JK25 CIRCUIT PACK

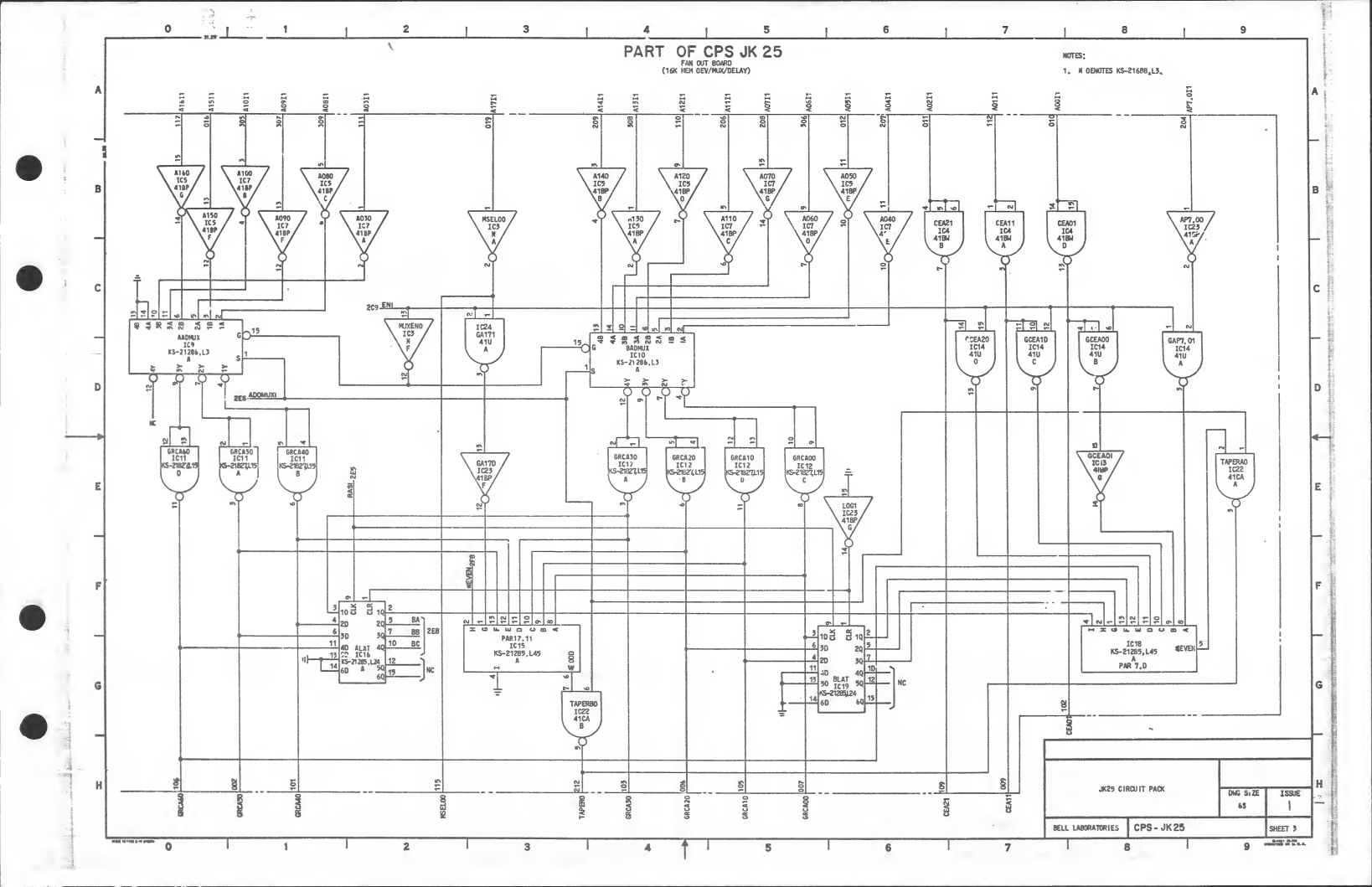
FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)
CIRCUIT

DWG SIZE	ISSUE
6S	1

BELL LABORATORIES | CPS-JK25 | 5 SHEETS

8262-570478


PART OF CPS JK25
FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)
SHEET NOTES:
1. N DENOTES KS-21680,L3.
JK25 CIRCUIT PACK
DWG SIZE
65
ISSUE
BELL LABORATORIES
CPS-JK25
SHEET 2


PART OF CPS JK 25
FAN OUT BOARD
(16K MEM OEV/MUX/DELAY)
NOTES:
1. M DENOTES KS-21688,L3.
A160 IC5 418P A
A150 IC5 418P F
A100 IC7 418P A
A090 IC7 418P F
A080 IC5 418P C
A030 IC7 418P E
MSEL00 IC9 M A
A140 IC9 418P B
A130 IC9 418P A
A120 IC9 418P D
A110 IC7 418P C
A070 IC7 418P D
A060 IC7 418P D
A050 IC9 418P C
A040 IC7 418P E
CEA21 IC4 418W B
CEA11 IC4 418W A
CEA01 IC4 418W D
AP7,00 IC23 41CA A
2C9 ENI
MUXEND IC3 M
IC24 GA171 41U A
AADMUX IC9 KS-21286,L3 A
BADMUX IC10 KS-21286,L3 A
GCEA20 IC14 41U D
GCEA11 IC14 41U C
GCEA00 IC14 41U B
GAP7,01 IC14 41U A
2E6 ADDMUXI
GRCA60 IC11 KS-21827,L15 D
GRCA50 IC11 KS-21827,L15 A
GRCA40 IC11 KS-21827,L15 B
GA17D IC23 418P F
GRCA30 IC12 KS-21827,L15 A
GRCA20 IC12 KS-21827,L15 B
GRCA10 IC12 KS-21827,L15 D
GRCA00 IC12 KS-21827,L15 C
GCEAOI IC13 418P B
TAPERA0 IC22 41CA A
LOGI IC23 418P C
RAM 22S
SEVEN 2F8
ALAT IC16 KS-21285,L24 A
2EB
PAR17,11 IC15 KS-21285,L45 A
NCOD
TAPERB0 IC22 41CA B
BLAT IC19 KS-21285,L24 A
IC18 KS-21285,L45 A PAR 7,D
SEVEN
CEA01
GRCA60
GRCA50
GRCA40
MSEL00
TAPERB0
GRCA30
GRCA20
GRCA10
GRCA00
CEA21
CEA11
JK25 CIRCUIT PACK
DWG SIZE
A3
ISSUE
1
BELL LABORATORIES
CPS-JK25
SHEET 3

PART OF CPS JK25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

COMPONENT LIST
INTEGRATED CIRCUIT

LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7		IC8		IC9		IC10		IC11		IC12		IC13		LOC
CODE	KS-21827,L15		KS-21827,L15		KS-21685,L3		41BW		41BP		KS-22038,L1		41BP		KS-22038,L1		KS-21286,L3		KS-21286,L3		KS-21827,L15		KS-21827,L15		41BP		CODE
ELEM																											ELEM
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	ID
A	REF0	2C4		2B7	MSELOO	3B3	CEA11	3B7	A130	3B4	CASOEL1	2D6	A010	3B2	ADDMUX1	2D5	AAOMUX	3D0	BAOMUX	3D4	GRCA50	3E1	GRCA30	3C4	GRW1	2E1	A
B	GRW0	2D0		2B7	RAS1	2C4	CEA21	3B7	A14F	3B4			A100	3B1							GRCA40	3E1	GRCA20	3E4	GRAS1	2F5	B
C		2B8	EN1	2C2	RA1	2B0		2B1	A080	3B1			A110	3B5								2B9	GRCA00	3E5	REFCK1	2C4	C
D	GCAS0	2E6	GRAS0	2C4	REF1	2B3	CEA01	3B8	A120	3B4			A040	3B5							GRCA60	300	GRC410	3E9		2B6	D
E					MEN0	2B2			A050	3B6			A040	3B6												2B6	E
F					MUXEN0	3C2			A150	3B0			A090	3B1											CLKEN1	2E2	F
G									A160	3B0			A070	3B5											GCEA01	3E8	G

LOC	IC14		IC15		IC16		IC17		IC18		IC19		IC20		IC21		IC22		IC23		IC24		LOC
CODE	41U		KS-21289,L45		KS-21285,L24		41U		KS-21289,L45		KS-21289,L24		KS-21289,L45		41CA		41CA		41BP		41U		CODE
ELEM																							ELEM
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	ID
A	GAP7.01	3E9					CLKEN0	2D2							MSELO	2D1	TAPERA0	3E9	AP7.00	3B9	GA171	3D3	A
B	GCEA00	3E8	PAR17.11	3G3	ALAT	3F2	RSELO	2F3	PAR7.0	3G8	BLAT	3G6	PAR10.8	2E7	RSEL1	2G3	TAPERB0	3G3	AP17.80	2C8	GP17.81	2D8	B
C	GCEA10	3E7					GRC1	2F5							SELRA0	2F1	UNSELERO	2G5	TS10	2C7		2B8	C
D	GCEA20	3E7					GCAS1	2F5								2B8	SELRC0	2G5		2B5	TSORME	2D7	D
E																			GA170	2B9			E
F																			L061	3E3			F
G																				3E6			G

CAPACITOR

DESIG	CODE
[24] C1-C24	KS-21901,L1 .1
[4] C25-C28	601A 5

TABLE 1

WIRE FANOUT BOARD TERMINAL

MODULE	J3 TO
0	115
1	019

JK25 CIRCUIT PACK		DWG SIZE	ISSUE
		A5	
BELL LABORATORIES	CPS-JK25	SHEET 4	

PART OF CPS JK25

CIRCUIT DESCRIPTION/TIMING

CIRCUIT DESCRIPTION

THE JK25 FAN-OUT-BOARD (FOB) IS USED AS AN ADDRESS AND CONTROL SIGNAL BUFFER BETWEEN A MEMORY CONTROLLER AND A MODULE OF MEMORY PLANES. A MODULE OF MEMORY PLANES THAT USE 16K RAMS IS DEFINED AS 128K WORDS. IN ADDITION, CONTROL MONITOR OUTPUTS ARE PROVIDED TO PERMIT VERIFICATION OF CIRCUIT OPERATION. ALL INPUTS AND OUTPUTS ARE +5 VOLT TTL COMPATIBLE.

THE 16K DYNAMIC MEMORY DEVICE REQUIRES A 14-BIT MULTIPLEXED ADDRESS AND TWO CLOCK PULSES TO ACHIEVE PROPER OPERATION. THE TIMING RELATIONSHIPS BETWEEN THE CLOCKS AND ADDRESSES CAN BE FOUND ON SHEET 8. THE JK25 CIRCUITRY MULTIPLEXES ADDRESS BITS A0911 THROUGH A1611 AND DRIVES THIS MULTIPLEXED INFORMATION TO THE MEMORY PLANES ON NETS GRCA00 THROUGH GRCA60. THE FIRST SEVEN ADDRESS BITS THAT ARE GATED THROUGH THE FOB ARE THE ROW ADDRESS BITS AND THE SECOND SEVEN ADDRESS BITS ARE THE COLUMN ADDRESS BITS. SINCE THE ADDRESSES ARE VALID ONLY FOR CERTAIN PORTIONS OF THE CYCLE, REGISTERS ARE PROVIDED TO LATCH THE ADDRESSES THAT ARE SENT TO THE MEMORY PLANES UNTIL A PARITY CHECK CAN BE PERFORMED ON THEM.

THE JK25 ADDRESS BUFFER CIRCUITRY IS CHECKED FOR ODD PARITY OVER A0011 THROUGH A0711 AND APT.011, AND FOR ODD PARITY OVER A0811 THROUGH A1711 AND A17.B11. AN ADDRESS PARITY ERROR IS INDICATED BY A LOW LEVEL ON OUTPUT TAPERO.

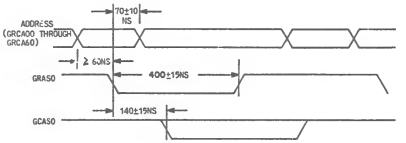
AS SHOWN IN TABLE 1, THE JK25 IS ENABLED BY HARDWIRING EITHER SIGNAL MSEL00 OR A1711 TO DECODING GATE MEN0. THE PRESENCE OF THE MODULE ENABLE SIGNAL, GATE EN1 HIGH, FORCES OPEN COLLECTOR OUTPUT MSEL0 TO THE LOW STATE. ALL INPUT ADDRESS BITS EXCEPT THE THREE LEAST SIGNIFICANT BITS (A0011 THROUGH A0211) ARE GATED THROUGH THE JK25 BY ENABLE GATE EN1. IN THE SELECTED STATE GATE MUXEN0 ENABLES THE MULTIPLEXORS AND ALLOWS ADDRESS BITS A0911 THROUGH A1611 TO BE MULTIPLEXED. THESE ADDRESS BITS ARE INVERTED AND APPEAR AT OUTPUTS GRCA00 THROUGH GRCA60. IN THE UNSELECTED CONDITION, THE GATED ADDRESS OUTPUTS ARE FORCED TO THE LOW STATE. THE UNGATED ADDRESS BITS, A0011 THROUGH A0211 ARE INVERTED AND APPEAR AT OUTPUTS CEA01 THROUGH CEA21, RESPECTIVELY, REGARDLESS OF THE STATE OF EN1.

TWO 70ns DELAY LINES PROVIDE THE TIMING RELATIONSHIPS BETWEEN THE ADDRESS MULTIPLEXING AND THE SECOND CLOCK PULSE (GCAS0) AND ALSO PROVIDES A GATING INPUT TO THE ADDRESS PARITY ERROR GATES (TAPERA0, TAPERB0).

SEVERAL MEMORY CONTROL SIGNALS ARE BUFFERED AND GATED THROUGH THE JK25. WHEN SELECTED, OUTPUT GRA0 FOLLOWS INPUT RA10. IN THE UNSELECTED CONDITION, GRA0 IS FORCED TO A HIGH-LEVEL STATE. OPEN COLLECTOR OUTPUT SELRA0 IS PROVIDED TO MONITOR THE STATE OF OUTPUT GRA0. INPUT RAS10 AND THE MODULE ENABLE SIGNAL CONTROL GRAS0. GCAS0 IS CONTROLLED BY THE MODULE ENABLE SIGNAL, EN1, THE REFRESH ENABLE GATE, REFQ, AND THE INPUT PULSE FROM THE DELAY LINE, CASDEL1. GCAS0 IS INACTIVE DURING ALL REFRESH CYCLES. OPEN COLLECTOR OUTPUT SELRC0 IS PROVIDED TO MONITOR THE STATES OF OUTPUTS GRAS0 AND CCAS0. IN ADDITION, OUTPUT UNSELER0 IS PROVIDED AND ASSUMES A LOW STATE IF EITHER GRAS0 OR GC... BECOMES ACTIVE (LOW) WHILE THE JK25 IS IN THE UNSELECTED STATE, THUS INDICATING AN ERROR. MAINTENANCE INPUT TS111 IS PROVIDED TO TEST THE INTEGRITY OF THIS GATING PATH.

REFRESH CONTROL INPUT RFFI0 IS PROVIDED TO FORCE JK25 TO THE ENABLED STATE INDEPENDENT OF ADDRESS BIT A1711 A NONINVERTED REPLICA OF REFI0 APPEARS AT OUTPUT REFQ. A HIGH LEVEL AT OPEN COLLECTOR OUTPUT RSEL1 INDICATES THE PRESENCE OF THE REFRESH STATE, THE REFQ OUTPUT ACTIVE (LOW), AND THE GCAS0 OUTPUT INACTIVE (HIGH).

JK25 TIMING EXAMPLE



JK25 CIRCUIT PACK		DWG SIZE 65	ISSUE /
BELL LABORATORIES	CPS-JK25		SHEET 9